Generic
NiCR PROM Family
53/63XXX-1 53/63XXX-2

Features/Benefit

- From 256 Bit to 8192 Bit memory
- 4-bit-wide and 8-bit-wide for byte oriented applications
- -1 series for standard performance
- -2 series for enhanced performanced
- Reliability proven nichrome fusible links (qualified for MIL-M-38510)
- PNP inputs for low input current
- Compatible pin configurations for upward expansion

Application

- Microprogram store
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 53/63XX series generic PROM family offers a wide selection of size and organizations. The 4-bit wide PROMs range from 256x4 to 2048x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 8-bit wide PROMs range from 32x8 to 1024x8 in a wide selection of package size including the space saving SKINNYDIP™ 24-pin .300 inch wide package. ALL PROMs have the same programming specifications allowing a single generic programmer.

3

The family features low input current PNP inputs, full Schottky clamping, three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Generic PROM Selection Guide

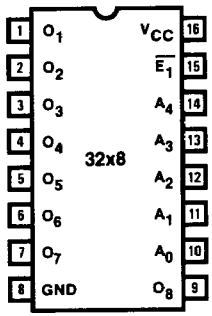
MEMORY			PACKAGE		DEVICE TYPE		OUTPUT
SIZE	ORGANIZATION		PINS	TYPE	COMMERCIAL	MILITARY	WIDTH
1K	256x4	OC TS	16	N, J, F, W	6300-1 6301-1	5300-1 5301-1	4-bit-wide
2K	512x4	OC TS	16	N, J, F, W	6305-1 6306-1	5305-1 5306-1	
4K	1024x4	OC TS	18	N, J	6352-1 6353-1, -2	5352-1 5353-1, -2	
8K	2048x4	OC TS	18	J	6388-1 6389-1, -2	5388-1 5389-1, -2	
¼K	32x8	OC TS	16	N, J, F, W	6330-1 6331-1	5330-1 5331-1	8-bit-wide
2K	256x8	OC TS	20	N, J, F	6308-1 6309-1	5308-1 5309-1	
		TS	24	J	6336-2		
4K	512x8	OC TS	24 (28)	N,JS*,F(L)	6340-1 6341-1, -2	5340-1 5341-1, -2	
		OC TS	20	N, J	6348-1 6349-1, -2	5348-1 5349-1, -2	
8K	1024x8	OC TS	24	N,J,JS*,F	6380-1, -2 6381-1, -2	5380-1, -2 5381-1, -2	

* JS is the .300 inch wide SKINNYDIP™ package.

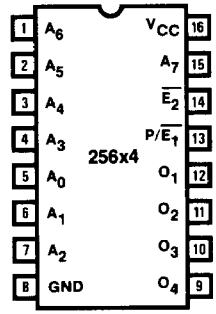
2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

Pin Configurations

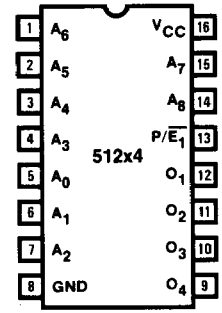
53/6330-1
53/6331-1



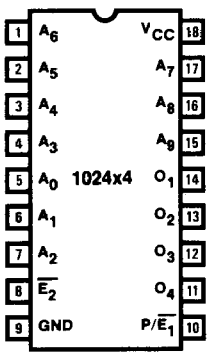
53/6300-1
53/6301-1



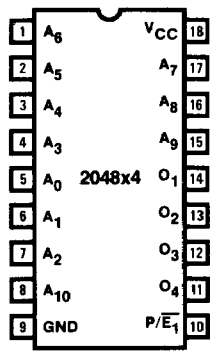
53/6305-1
53/6306-1



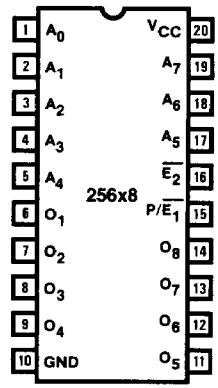
53/6352-1
53/6353-1, -2



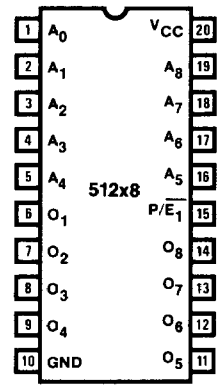
53/6388-1
53/6389-1, -2



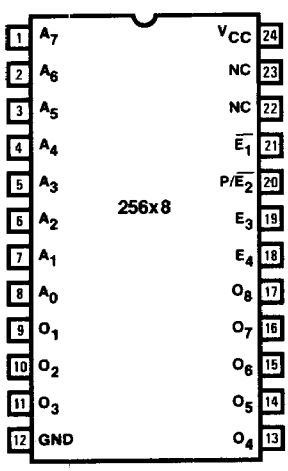
53/6308-1
53/6309-1



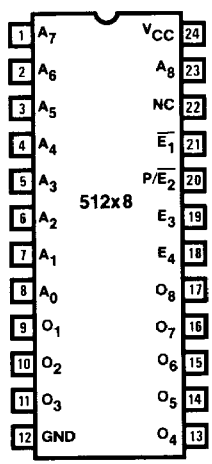
53/6348-1
53/6349-1, -2



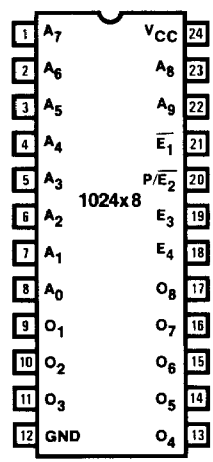
6336-2



53/6340-1
53/6341-1, -2



53/6380-1, -2
53/6381-1, -2



Absolute Maximum Ratings

Supply voltage V_{CC} ..... -0.5V to 7V
Input voltage ..... -1.5V to 7V
Off-state output voltage ..... -0.5V to 5.5V
Storage temperature range ..... -65°C to + 150°C

Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
T_A	Operating free-air temperature	-55		125	0		75	°C

3

Electrical Characteristics Over Operating Conditions

SYMBOL	PARAMETER	TEST CONDITIONS			-1 SERIES MIN	-1 SERIES MAX	-2 SERIES MIN	-2 SERIES MAX	UNIT
V_{IL}	Low-level input voltage					0.8		0.8	V
V_{IH}	High-level input voltage				2		2		V
V_{IC}	Input clamp voltage	V_{CC} = MIN	I_I = -18mA			-1.5		-1.5	V
I_{IL}	Low-level input current	V_{CC} = MAX	V_I = 0.45V			-0.25		-0.25	mA
I_{IH}	High-level input current	V_{CC} = MAX	V_I = 4.5V (Program pin) V_I = V_{CC} MAX (Other pins)			40		40	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OL} = 12mA			0.5		0.5	V
			COM I_{OL} = 16mA						
V_{OH}	High-level output voltage *	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	MIL I_{OH} = -2mA		2.4		2.4		V
			COM I_{OH} = -3.2mA						
I_{OZL}	Off-state output current *	V_{CC} = MAX	V_O = 0.5V			-100		-40	μA
I_{OZH}			V_O = 2.4V			100		40	μA
I_{CEX}	Open collector output current	V_{CC} = MAX	V_O = 2.4V			100		40	μA
			V_O = 5.5V					100	
I_{OS}	Output short-circuit current*†	V_{CC} = 5V	V_O = 0V		-20	-90	-20	-90	mA
I_{CC}	Supply current	V_{CC} = MAX All inputs grounded. All outputs open	'30. '31.			125			mA
			'00. '01.			130			
			'05. '06.			130			
			'08. '09. '36.			155		155	
			'40, '41, '48, '49	MIL		155		175	
				COM		155		155	
			'52, '53			175		140	
			'88, '89	MIL		170		170	
				COM		170		155	
			80, 81	MIL		175		175	
				COM		175		170	

* Thre-state only.
† Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Switching Characteristics

Over Commercial Operating Conditions

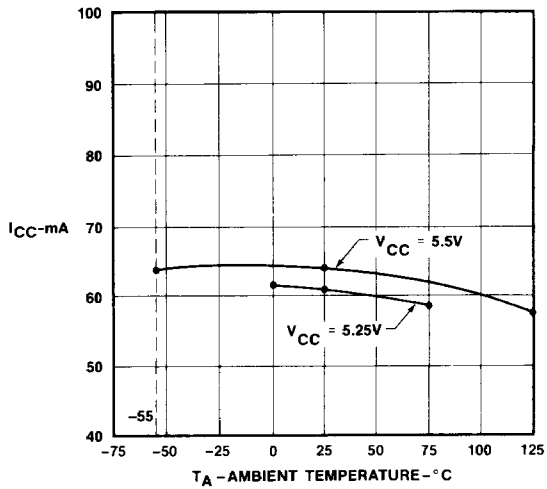
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	R1 (Ω)	R2 (Ω)
6300-1, 6301-1	55	30	300	600
6305-1, 6306-1	60	30		
6308-1, 6309-1	70	30		
6330-1, 6331-1	50	30		
6336-2	70	30		
6340-1, 6341-1	70	30		
6341-2	55	30		
6348-1, 6349-1	70	30		
6349-2	55	30		
6352-1, 6353-1	60	30		
6353-2	50	30		
6388-1, 6389-1	70	30		
6389-2	55	30		
6380-1, 6381-1	90	40		
6380-2	70	30		
6381-2	55	30		

Over Military Operating Conditions

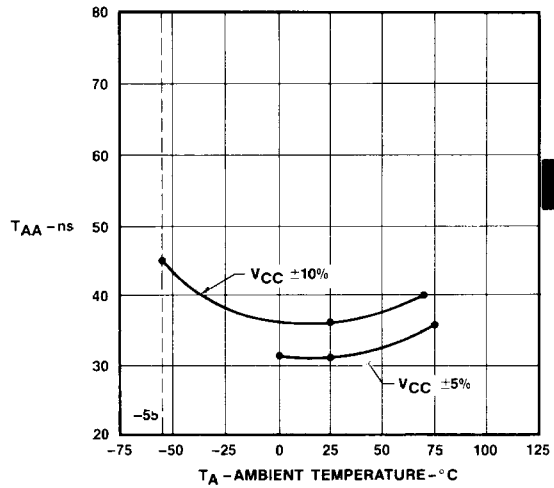
DEVICE TYPE	t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} AND t_{ER} (ns) ENABLE ACCES AND RECOVERY TIME	CONDITIONS (See standard test load)	
	MAX	MAX	R1 (Ω)	R2 (Ω)
5300-1, 5301-1	75	40	375	750
5305-1, 5306-1	75	40		
5308-1, 5309-1	80	40		
5330-1, 5331-1	60	40		
5336-2	80	40		
5340-1, 5341-1	80	40		
5341-2	70	40		
5348-1, 5349-1	80	40		
5349-2	70	40		
5352-1, 5353-1	75	40		
5353-2	65	30		
5388-1, 5389-1	100	40		
5389-2	70	40		
5380-1, 5381-1	125	40		
5380-2	90	40		
5381-2	70	40		

53/6331

Typical I_{CC} vs Temperature



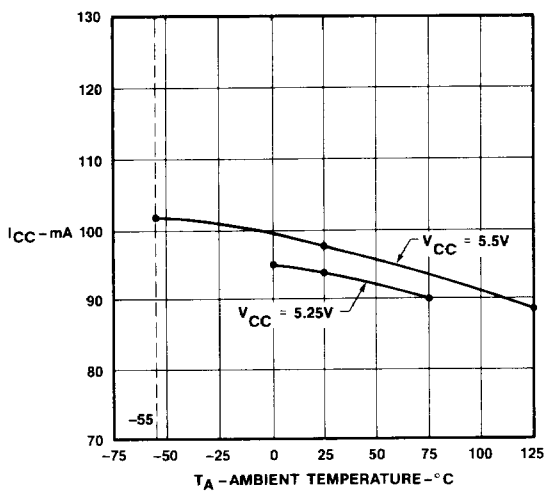
Typical T_{AA} vs Temperature



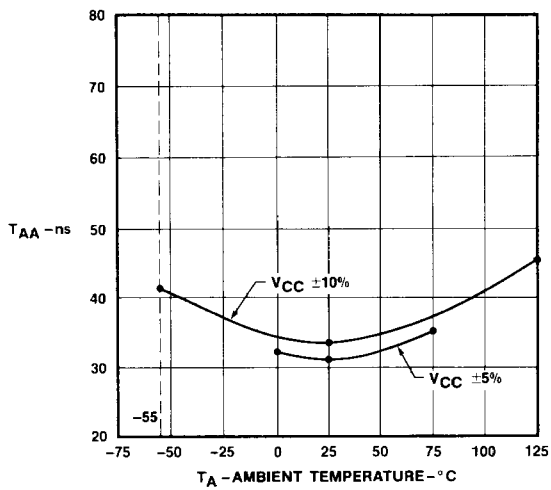
3

53/6301

Typical I_{CC} vs Temperature

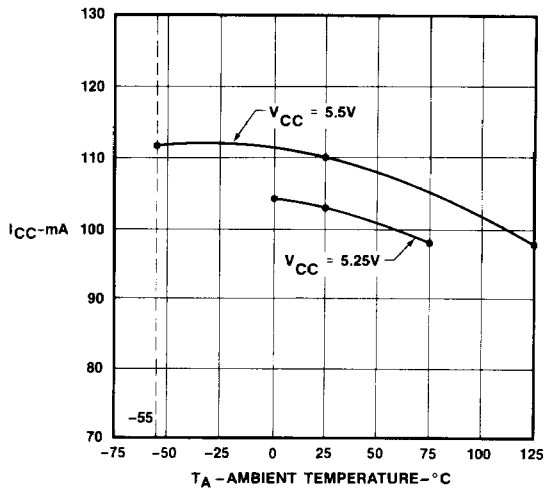


Typical T_{AA} vs Temperature

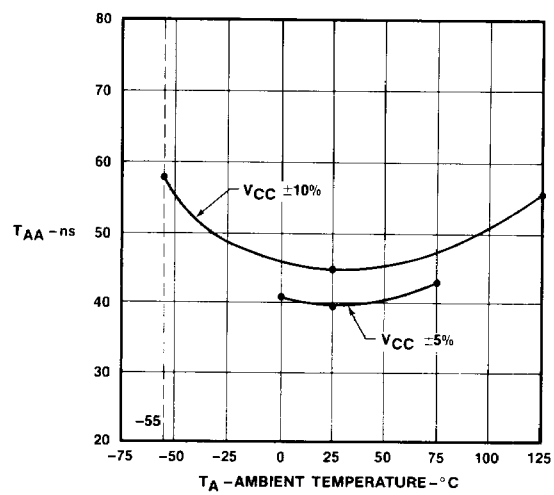


53/6306

Typical I_{CC} vs Temperature

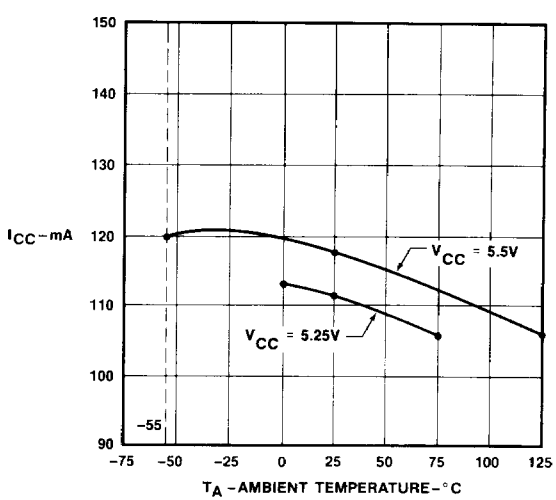


Typical T_{AA} vs Temperature

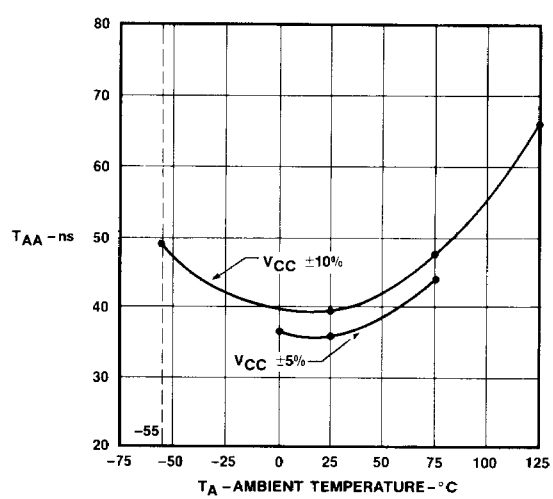


53/6309

Typical I_{CC} vs Temperature

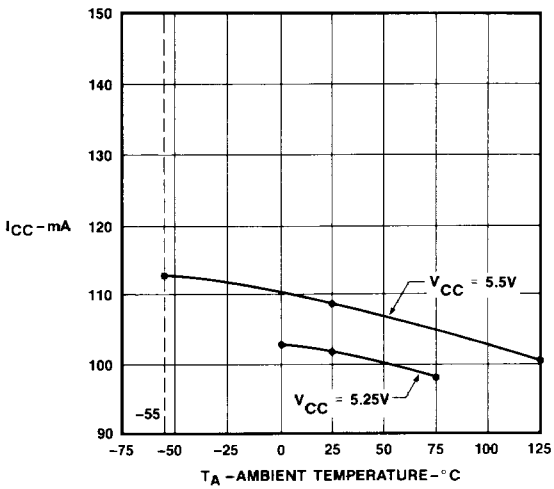


Typical T_{AA} vs Temperature

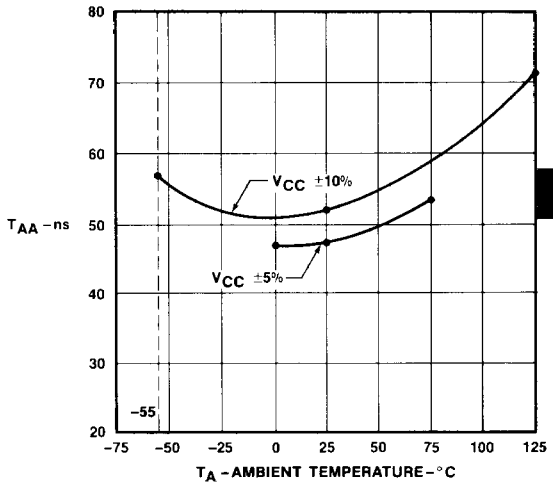


53/6336
53/6341
53/6349

Typical I_{CC} vs Temperature



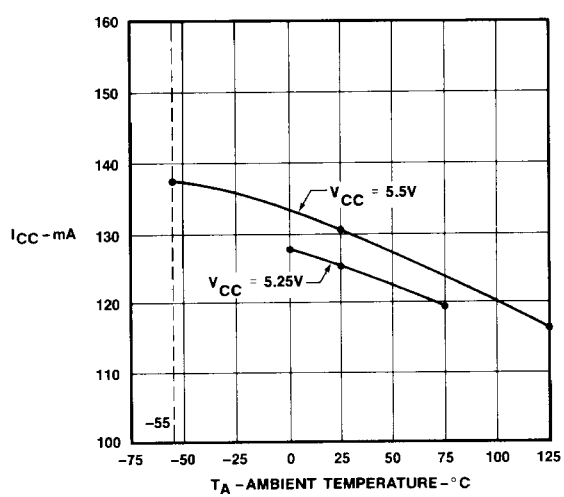
Typical T_{AA} vs Temperature



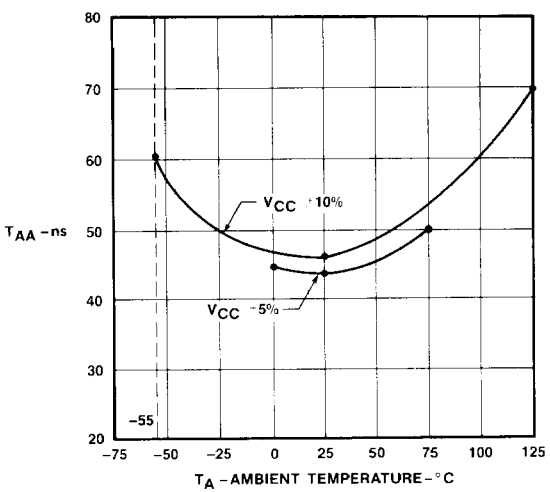
3

53/6353

Typical I_{CC} vs Temperature

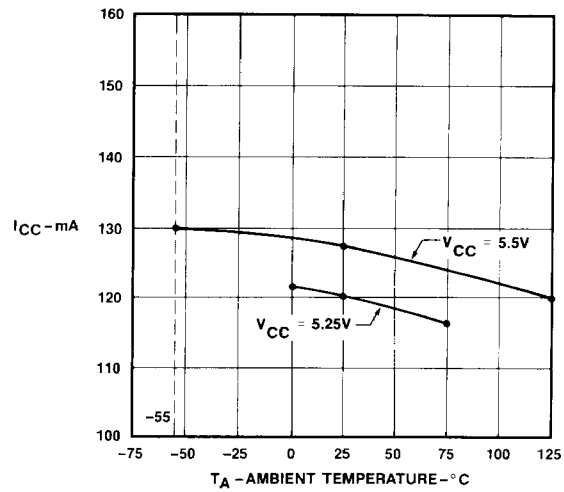


Typical T_{AA} vs Temperature

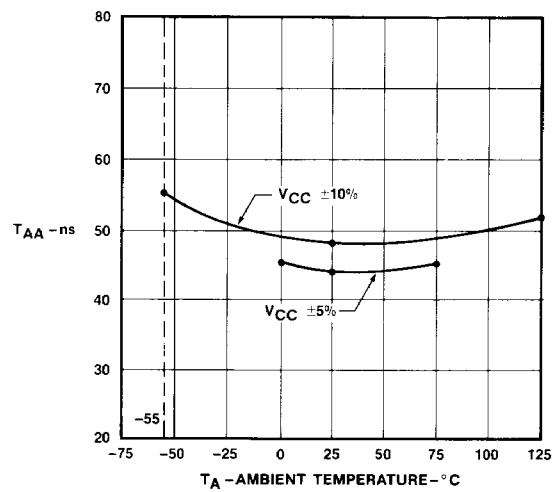


53/6389

Typical I_{CC} vs Temperature

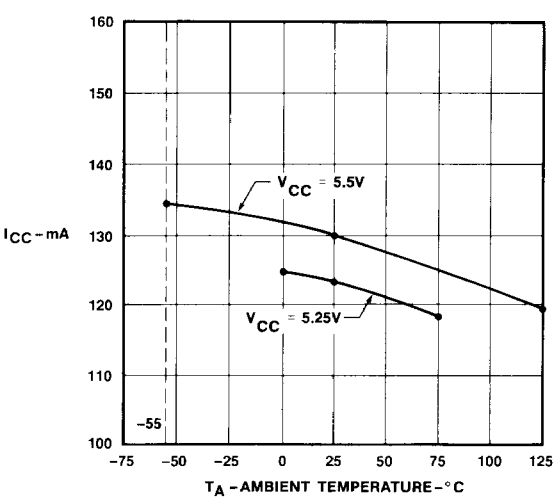


Typical T_{AA} vs Temperature

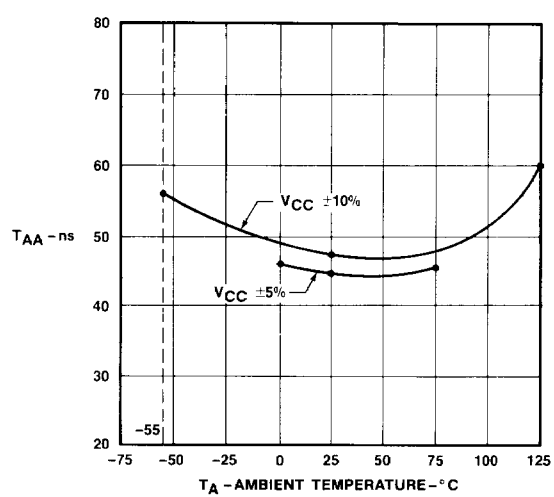


53/6381

Typical I_{CC} vs Temperature

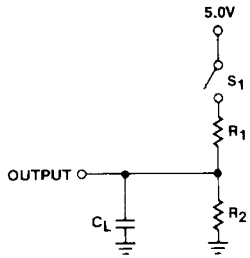


Typical T_{AA} vs Temperature



NOTE: Typical characteristic curves are for three-state devices. Equivalent open collector devices decrease in I_{CC} approximately 10 mA and increase in T_{AA} approximately 6 ns.

Switching Test Load

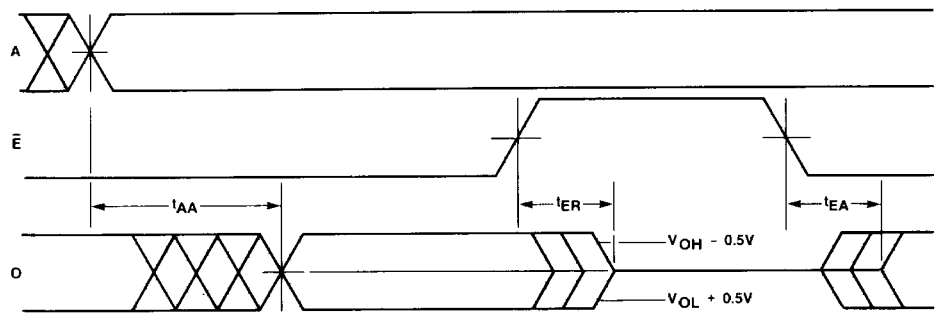


Definition of Timing Diagram

WAVEFORM	INPUTS	OUTPUTS
	DON'T CARE; CHANGE PERMITTED	CHANGING; STATE UNKNOWN
	NOT APPLICABLE	CENTER LINE IS HIGH IMPEDANCE STATE
	MUST BE STEADY	WILL BE STEADY

3

Definition of Waveforms



NOTES: 1. Input pulse amplitude 0V to 3.0V.

2. Input rise and fall times 2-5ns from 1.0V to 2.0V.

3. Input access measured at the 1.5V level.

4. t_{AA} is tested with switch S_1 closed, C_L = 30pF and measured at 1.5V output level.

5. For open collector devices. TEA and TER are measured at the 1.5V output level with S_1 closed and C_L = 30pF.

6. For three-state devices, TEA is measured at the 1.5V output level with C_L = 30pF. S_1 is open for high impedance to "1" test and closed for high impedance to "0" test.

   TER is tested with C_L = 5pF. S_1 is open for "1" to high impedance test, measured at V_{OH} - 0.5V output level; S_1 is closed for "0" to high impedance test measured at V_{OL} + 0.5V output level.

Commercial Programmers

Monolithic Memories PROMs are designed and tested to give a programming yield greater than 97%. If your programming yield is lower, check you programmer. It may not be properly calibrated. (See Figure 1).

Programming is final manufacturing—it must be quality-controlled. Equipment must be calibrated as a regular routine, ideally under the actual conditions of use. Each time a new board or a new programming module is inserted, the whole system should be checked. Both timing and voltages must meet published specifications for the device.

Remember—The best PROMs available can be made unreliable by improper programming techniques.

PROM PROGRAMMING EQUIPMENT INFORMATION

SOURCE AND LOCATION		
	Data I/O Corp. P.O. Box 308 Issaquah, WA 98027	Digelec Inc. 7335 E. Acoma DR Suite 103 Scottsdale, AZ 85260
	Kontron Electronic, Inc. 630 Price Ave. Redwood City, CA 94036	

NiCr PROM
Programming Instructions
53/63XX

Description

The 53/63XX Generic PROM Family is manufactured with outputs high in all storage locations. To make an output low at A particular word, a nichrome fusible link must be opened. This procedure is called programming.

Programming Procedure (See Figure 1)

1. Apply the desired address to the inputs.
2. Enable Inputs may be left at any state. *
3. Apply 5.5V to V_{CC}.
4. Apply V_{PP} to the program pin. (This step is not used on the 32x8 PROM) *
5. Apply V_{OUT} to the output to be programmed.
6. Remove V_{OUT}.
7. Remove V_{PP}.
8. Verification may be performed after each bit or word or after completing the programming of all memory locations.

In order to avoid misprogramming the PROM only one output at time is to be programmed. Outputs not being programmed should be connected to V_{CC} via 5K Ω resistors.

* The 5330/1 and 6330/1 do not have a program pin. For these devices the output only is used in programming a particular selected bit and the device must be in the disabled state.

Verification Procedure (See Figure 2)

1. Enable the device.
2. To verify low-state:
   - 2A. Apply an address where the output should be low.
   - 2B. Apply 4.2V to V_{CC}.
   - 2C. Load the output with I_{OL} = 12 mA.
   - 2D. Check that the output is less than 0.8V.
3. To verify High-state:
   - 3A. Apply an address where the output should be high.
   - 3B. Apply 6V to V_{CC}.
   - 3C. Load the output with I_{OH} = −0.3 mA.
   - 3D. Check that the output is higher than 4.5V.

3

Programming Parameters Do not test these parameters or you will program the device.

SYMBOL	PARAMETER	CONDITIONS TA = +25° C	FIGURE	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
t_R	Slew rate of Programming Pulses†			0.3		0.5	V/μs
V_{CCP}	VCC During Programming			5.4	5.5	5.6	V
	Maximum Duty Cycle					25	%
V_{PP}	Programming Voltage on Program Pin *		1	27		33	V
V_{OUT}	Programming Voltage on Output Pin *		1	20		26	V
t_{D1}	Delay between VPP and VOUT		1	0	10	20	μs
t_{D2}				0	0.5	1	
t_p	Pulse width of V_{OUT}		1	10		40	μs
V_{OLV}	VOL during verification	Chip enabled IOL = 12 mA VCC = 4.2V	2			0.8	V
V_{OHV}	VOH during verification	Chip enabled IOH = 0.3 mA VCC = 6V	2	4.5			V

*Voltage supply must be capable of supplying at least 240 mA.

†Leading edge of VPP and VOUT

2175 Mission College Boulevard, Santa Clara, CA 95050 Tel: (408) 970-9700 TWX: 910-338-2376 TWX: 910-338-2374

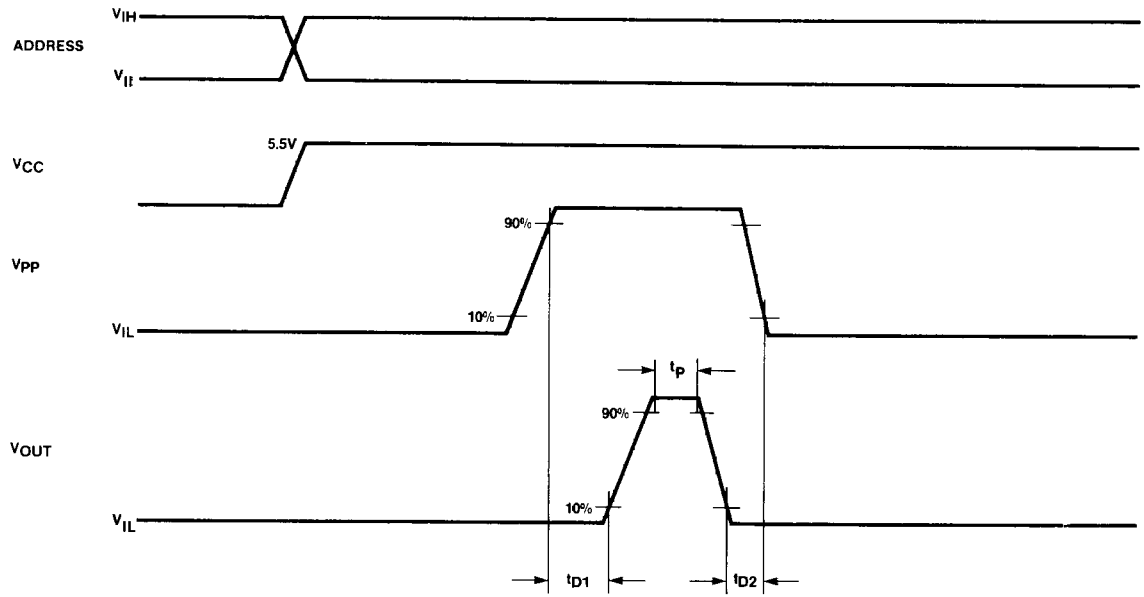


Figure 1. Programming Timing Diagram

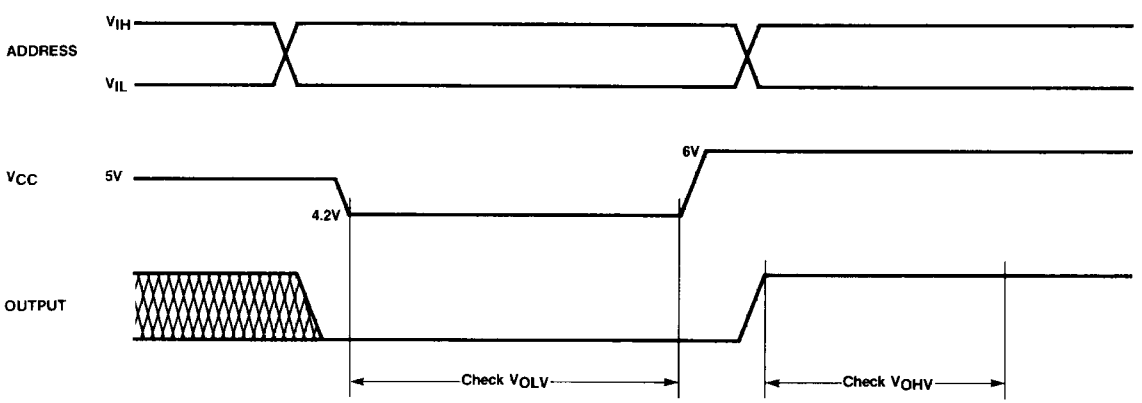


Figure 2. Verification Timing Diagram

Optimized Programming Algorithm

1. Pulse all fuses to be programmed with single, minimum voltage programming pulses (line 1 in the table).
2. Verify all fuses at low VCC (4.2V). During this step, unprogrammed fuses are pulsed up to eight more times (see table).
3. Re-verify at low VCC (4.2V) and high VCC (6V).

PULSE NUMBER	PROGRAM PIN VOLTAGE	OUTPUT VOLTAGE
1 to 3	27V	20V
4 to 6	30V	23V
7 to 9	33V	26V