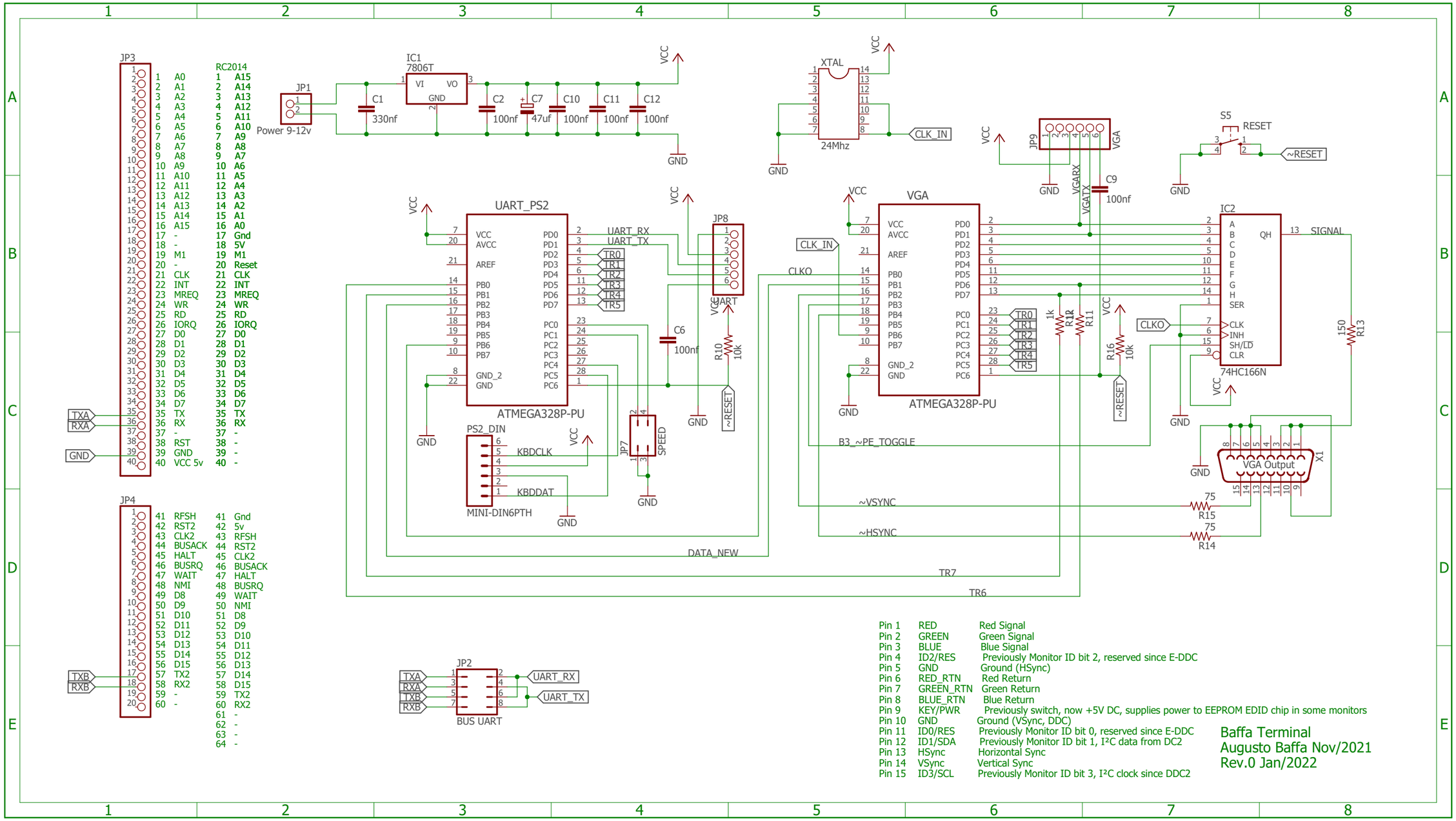
JP3
RC2014
1 A0 1 A15
2 A1 2 A14
3 A2 3 A13
4 A3 4 A12
5 A4 5 A11
6 A5 6 A10
7 A6 7 A9
8 A7 8 A8
9 A8 9 A7
10 A9 10 A6
11 A10 11 A5
12 A11 12 A4
13 A12 13 A3
14 A13 14 A2
15 A14 15 A1
16 A15 16 A0
17 - 17 Gnd
18 - 18 5V
19 M1 19 M1
20 - 20 Reset
21 CLK 21 CLK
22 INT 22 INT
23 MREQ 23 MREQ
24 WR 24 WR
25 RD 25 RD
26 IORQ 26 IORQ
27 D0 27 D0
28 D1 28 D1
29 D2 29 D2
30 D3 30 D3
31 D4 31 D4
32 D5 32 D5
33 D6 33 D6
34 D7 34 D7
35 TX 35 TX
36 RX 36 RX
37 - 37 -
38 RST 38 -
39 GND 39 -
40 VCC 5v 40 -
TXA
RXA
GND
JP4
41 RFSH 41 Gnd
42 RST2 42 5v
43 CLK2 43 RFSH
44 BUSACK 44 RST2
45 HALT 45 CLK2
46 BUSRQ 46 BUSACK
47 WAIT 47 HALT
48 NMI 48 BUSRQ
49 D8 49 WAIT
50 D9 50 NMI
51 D10 51 D8
52 D11 52 D9
53 D12 53 D10
54 D13 54 D11
55 D14 55 D12
56 D15 56 D13
57 TX2 57 D14
58 RX2 58 D15
59 - 59 TX2
60 - 60 RX2
61 -
62 -
63 -
64 -
TXB
RXB
JP1
Power 9-12v
IC1
7806T
VI
VO
GND
C1
330nf
C2
100nf
C7
47uf
C10
100nf
C11
100nf
C12
100nf
VCC
GND
XTAL
24Mhz
CLK_IN
JP9
VGA
VGARX
VGATX
C9
100nf
S5
RESET
~RESET
UART_PS2
VCC
AVCC
AREF
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
GND_2
PD0
PD1
PD2
PD3
PD4
PD5
PD6
PD7
PC0
PC1
PC2
PC3
PC4
PC5
PC6
UART_RX
UART_TX
TR0
TR1
TR2
TR3
TR4
TR5
ATMEGA328P-PU
JP8
UART
C6
100nf
R10
10k
~RESET
PS2_DIN
KBDCLK
KBDDAT
MINI-DIN6PTH
JP7
SPEED
DATA_NEW
TR7
TR6
VGA
CLKO
R11
R12
1k
R16
10k
B3_~PE_TOGGLE
~VSYNC
~HSYNC
IC2
74HC166N
A
B
C
D
E
F
G
H
SER
CLK
INH
SH/LD
CLR
QH
SIGNAL
150
R13
VGA Output
X1
75
R15
75
R14
JP2
BUS UART
Pin 1 RED Red Signal
Pin 2 GREEN Green Signal
Pin 3 BLUE Blue Signal
Pin 4 ID2/RES Previously Monitor ID bit 2, reserved since E-DDC
Pin 5 GND Ground (HSync)
Pin 6 RED_RTN Red Return
Pin 7 GREEN_RTN Green Return
Pin 8 BLUE_RTN Blue Return
Pin 9 KEY/PWR Previously switch, now +5V DC, supplies power to EEPROM EDID chip in some monitors
Pin 10 GND Ground (VSync, DDC)
Pin 11 ID0/RES Previously Monitor ID bit 0, reserved since E-DDC
Pin 12 ID1/SDA Previously Monitor ID bit 1, I²C data from DC2
Pin 13 HSync Horizontal Sync
Pin 14 VSync Vertical Sync
Pin 15 ID3/SCL Previously Monitor ID bit 3, I²C clock since DDC2
Baffa Terminal
Augusto Baffa Nov/2021
Rev.0 Jan/2022